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| **Course Name:** | **Digital Design Laboratory** | **Semester:** | **III** |
| **Date of Performance:** | **9 /10 /2023** | **Batch No:** | **C-2** |
| **Faculty Name:** |  | **Roll No:** | **16010122267** |
| **Faculty Sign & Date:** |  | **Grade/Marks:** | **\_\_\_/25** |

**Experiment No: 8**

**Title: 1-bit adder on VHDL**

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| **Aim and Objective of the Experiment:** |
| To implement 1-bit adder on VHDL |

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| **COs to be achieved:** |
| **CO4**: Implement digital networks using VHDL |

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| **Tools used:** |
| Quartus, ModelSim |

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| **Theory:** |
| A 1-bit adder, a fundamental component of digital circuits, performs binary addition of two 1-bit numbers. It utilizes logic gates to generate the sum and carry-out outputs. A half-adder adds two bits without considering the carry from the previous stage, while a full-adder accounts for the carry input.  Using VHDL, a hardware description language, the 1-bit adder can be designed as a combinational circuit. VHDL facilitates the creation of a structural and behavioral description of the adder. In practice, this simple unit serves as a building block for constructing larger multi-bit adders, enabling arithmetic operations in microprocessors and digital systems. |

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| **Implementation Details** |
| **Code:** |
| **Post Lab Subjective/Objective type Questions:** |
| 1. How can 1-bit adder be used to implement a 4-bit adder?   **Ans:**  A 1-bit adder, also known as a half-adder, can be used as a building block to create a 4-bit adder. To build a 4-bit adder, you would cascade four 1-bit adders together, with each 1-bit adder handling one bit of the input and output  1. **Define the Inputs and Outputs:** A 4-bit adder takes two 4-bit inputs, A and B, and produces a 4-bit sum (S) and a carry-out (Cout).  2**. Cascading Half-Adders:** To add two 4-bit numbers, you start by adding the least significant bits (LSBs) first. So, you connect the LSBs of A and B to the inputs of the first half-adder, resulting in a 1-bit sum (S0) and a carry-out (Cout0). The sum S0 is the LSB of the output, and Cout0 is then carried to the next stage.  3. **Repeat the Process:** Connect the next bit (bit 1) of A and B to the inputs of the second half-adder. Additionally, connect Cout0 from the first half-adder to one of the inputs of the second half-adder. This simulates adding bit 1 along with the carry-out from the previous stage. You get another 1-bit sum (S1) and carry-out (Cout1).  4. **Continue Cascading:** Continue this process for bits 2 and 3, connecting them to the inputs of the third and fourth half-adders and taking carry-outs from the previous stages. This will give you S2, S3, Cout2, and Cout3.  5. **Final Output:** The final 4-bit sum (S) is composed of S3, S2, S1, and S0 from the individual half-adders, while the carry-out Cout3 represents the carry-out of the entire 4-bit addition.   1. What is VHDL used for?   **Ans:**  VHDL serves a dual purpose in the realm of electronic design, as it can be employed for both hardware design and the generation of test entities to assess the hardware's functionality. It is utilized as a preferred input format by numerous Electronic Design Automation (EDA) tools, encompassing synthesis solutions like Quartus® Prime Integrated Synthesis, simulation software, and formal verification tools. |
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| **Conclusion:** |
| Through this experiment, we successfully implemented 1 bit adder on VHDL. |

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| **Signature of faculty in-charge with Date:** |